The Analog Mixed Signal Company

ZMD31050

Advanced Differential Sensor Signal Conditioner

Data Sheet

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Data Sheet

Advanced Differential Sensor Signal Conditioner

ZMD31050

Brief Description

ZMD31050 is a CMOS integrated circuit for highly-accurate amplification and sensor-specific correction of bridge sensor signals. The device provides digital compensation of sensor offset, sensitivity, temperature drift and non-linearity by a 16-bit RISC micro controller running a correction algorithm with correction coefficients stored in non-volatile EEPROM.

The ZMD31050 accommodates virtually any bridge sensor (e.g. piezo-resistive, ceramic-thick film or steel membrane based). In addition, the IC can interface a separate temperature sensor.

The bi-directional digital interfaces (I^2C, SPI, ZACwire™) can be used for a simple PC-controlled one-shot calibration procedure, in order to program a set of calibration coefficients into an on-chip EEPROM. Thus a specific sensor and a ZMD31050 are mated digitally: fast, precise and without the cost overhead associated with laser trimming, or mechanical potentiometer methods.

Benefits

- No external trimming components required
- PC-controlled configuration and calibration via digital bus interface - simple, low cost
- High accuracy (±0.1% FSO @ -25°C to 85°C; ±0.25% FSO @ -40°C to 125°C)

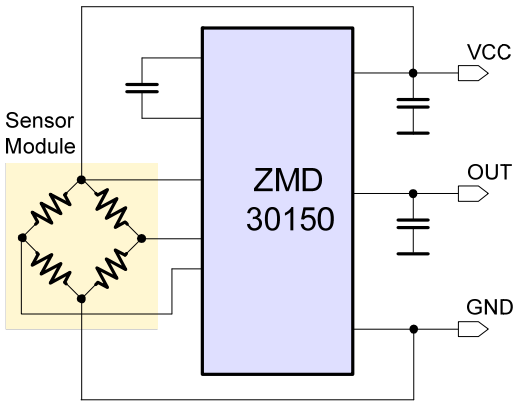
Available Support

- Application kit (SSOP16 samples, calibration PCB, calibration software, technical documentation)
- Support for industrial mass calibration
- Quick circuit customization for large production volumes

Features

- Digital compensation of sensor offset, sensitivity, temperature drift and non-linearity
- Accommodates nearly all bridge sensor types (signal spans from 1 up to 275mV/V processable)
- Digital one-shot calibration: quick and precise
- Selectable compensation temperature T1 source: bridge, thermistor, internal diode or external diode
- Output options: voltage (0V to 5V), current (4mA to 20mA), PWM, I^2C, SPI, ZACwire™ (one-wire-interface), alarm
- Adjustable output resolution (up to 15 bits) versus sampling rate (up to 3.9kHz)
- Selectable bridge excitation: ratiometric voltage, constant voltage or constant current
- Input channel for separate temperature sensor
- Sensor connection and common mode check
  (Sensor aging detection)
- Operation temperature -40 to +125°C (-40 to +150°C derated, depending on product version)
- Supply voltage +2.7V to +5.5V
- Available in SSOP16 or as die

ZMD31050 Overview



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1.1. Absolute Maximum Ratings

Table 1.1 Absolute Maximum Ratings

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
1.1.1	Digital Supply Voltage	VDD_{AMR}	-0.3		6.5	V DC	To VSS
1.1.2	Analog Supply Voltage	$VDDA_{AMR}$	-0.3		6.5	V DC	To VSS
1.1.3	Voltage at all analog and digital I/O – Pins	$V_{A\_I/O}$, $V_{D\_I/O}$	-0.3		VDDA +0.3	V DC	Exception see 1.1.4
1.1.4	Voltage at Pin FBP	V_{FBP_AMR}	-1.2		VDDA +0.3	V DC	4 mA to 20mA – Interface
1.1.5	Storage temperature	T_{STG}	-45		150	°C	

1.2. Operating Conditions [1] (Voltages related to VSS)

Table 1.2 Operating Conditions

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
1.2.1	Ambient temperature advanced performance	T_{ADV}	-25		85	°C	TQI = -25 to 85°C TQC = 0 to 70°C
1.2.2.1	Ambient temperature Automotive range	T_{AMB_TQA}	-40		125	°C	
1.2.2.2	Ambient temperature Extended automotive range	T_{AMB_TQE}	-40		150	°C	Operation life time < 1000h @ 125 to 150°C
1.2.3	Ambient temperature EEPROM programming	T_{AMB_EEP}	-25		85	°C	
1.2.4	EEPROM programming cycles				100		
1.2.5	Data retention (EEPROM)				15	a	Averaged temp < 85°C
1.2.6	Analog Supply Voltage	VDDA	2.7		5.5	V DC	Ratiometric mode
1.2.7	Analog Supply Voltage advanced performance	$VDDA_{ADV}$	4.5		5.5	V DC	Ratiometric mode
1.2.8	Digital Supply Voltage	VDD	- 2.7		1.05 -	VDDA V DC	External powered
1.2.9	External Supply Voltage	V_{SUPP}	VDDA + 2V		[2]	V DC	Voltage regulator mode with ext. JFET
1.2.10	Common mode input range	V_{IN_CM}	0.21		0.76	VADC_ REF	Depends on gain adjust, refer chapter 2.3.1.
1.2.11	Input Voltage Pin FBP	V_{IN_FBP}	-1		VDDA	V DC	
1.2.12	Sensor Bridge Resistance *	R_{BR} R_{BR_CL}	3.0 [1] 5.0		25.0 25.0	kΩ kΩ	Full temperature range CurrentLoop-IF 4 to 20mA

[1] Default configuration: 2nd order AD-conversion, 13Bit Resolution, gain >=210, fclk<=2.25MHz
[2] Maximum depending on breakdown voltage of external JFET, notice application hints in related application note.

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
1.2.13	Reference Resistor for Bridge Current Source *	RBR_REF	0.07			RBR	Leads to IBR = VDDA / (16·RBR_REF)
1.2.14	Stabilization Capacitor *	CVDDA	50	100	470	nF	Between VDDA and VSS, external
1.2.15	VDD Stabilization Capacitor *	CVDD	0 [2]	100	470	nF	Between VDD and VSS, external
1.2.16	Maximum allowed load capacitance at OUT3	CL_OUT			50	nF	Output Voltage mode
1.2.17	Minimum allowed load resistance	RL_OUT	2			kΩ	Output Voltage mode
1.2.18	Maximum allowed load capacitance at VGATE	CL_VGATE			10	nF	Summarized to all potentials

1.3. Build In Characteristics

Table 1.3 Build In Characteristics

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
1.3.1	Selectable Input Span, Pressure Measurement	V_{IN_SP}	2		280	mV/V	Refer chapter 2.3.1.
1.3.2	Analog Offset Comp Range (6 Bit setting)		-20 -25		20 25	count	ADJREF:BCUR=7
1.3.3	A/D Resolution	r_{ADC}	9		15	Bit	3 Bit setting [4]
1.3.4	D/A Resolution	r_{DAC}		11		Bit	@ analogue output
1.3.5	PWM - Resolution	r_{PWM}	9		12	Bit	
1.3.6	Bias current for external temperature diodes	I_{TS}	8	18	40	µA	
1.3.7	Sensitivity internal temperature diode	ST_{T_SI}	2800	3200	3600	ppm f.s. /K	Raw values - without conditioning
1.3.8	Clock frequency	f_{CLK}	1 *	2	4 *	MHz	guaranteed adjustment range

* No measurement in mass production, parameter is guarantied by design and/or quality observation
[1] No limitations with an external connection between VDDA and VBR
[2] Lower stabilization capacitors can increase noise level at the output
[3] If used, consider special requirements of ZACwire™ single wire interface stated in “Functional Description” chapter 4.3
[4] Resolution of 15bit is not applicable for 1st order ADC and not recommended for sensors with high nonlinearity behaviour

1.3.9 Cycle Rate versus A/D-Resolution *

(linear related to master clock frequency1 - values calculated at exact 2 MHz)

Table 1.4 Cycle Rate versus A/D-Resolution

ADC Order	Resolution	Conversion Cycle fCYC	
OADC	rADC Bit	fCLK=2MHz	fCLK=2.25MHz
		Hz	Hz
1	9	1302	1465
	10	781	879
	11	434	488
	12	230	259
	13	115	129
	14	59	67
2	11	3906	4395
	12	3906	4395
	13	1953	2197
	14	1953	2197
	15	977	1099

1.3.10 PWM Frequency *

Table 1.5 PWM Frequency

PWM	PWM Freq./Hz at 2 MHz Clock1				PWM Freq./Hz at 2.25 MHz Clock2			
Resolution	Clock Divider				Clock Divider			
rPWM [Bit]	1	0,5	0,25	0,125	1	0,5	0,25	0,125
9	3906	1953	977	488	4395	2197	1099	549
10	1953	977	488	244	2197	1099	549	275
11	977	488	244	122	1099	549	275	137
12	488	244	122	61	549	275	137	69

* No measurement in mass production, parameter is guarantied by design and/or quality observation
[1] Internal RC – Oscillator: coarse adjustment to1, 2 and 4 MHz, fine tuning +/- 25% , external clock is also possible
[2] Internal RC – Oscillator: coarse adjustment to1.125, 2.25 and 4.5 MHz, fine tuning +/- 25% , external clock is also possible

1.4. Electrical Parameters [4] (Voltages related to VSS)

Table 1.6 Electrical Parameters

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
1.4.1. Supply / Regulation							
1.4.1.1	Supply current	I_{SUPP}		2.5	4	mA	Without bridge and load current, f_{CLK}≤2.4MHz, Bias-Adjust≤4
1.4.1.2	Supply current for current loop	I_{SUPP_CL}		2.0	2.75		Without bridge current, f_{CLK}≤1.2MHz, Bias-Adjust≤1 [1]
1.4.1.2	Temperature Coeff. Voltage Reference *	TC_{REF}	-200	±50	200	ppm/K	
1.4.2. Analog Front End							
1.4.2.1	Parasitic differential input offset current *	I_{IN_OFF}	-2 to -10		2 to 10	nA	Temp. range 5.2.2., T_{ADV}
1.4.3. DAC & Analog Output (Pin OUT)							
1.4.3.1	Output signal range	V_{OUT_SR}	0.025		0.975	VDDA	Voltage Mode, R_{LOAD} > 2K□ $VDDA_{ADV}$,T_{ADV} [2]
1.4.3.2	Output DNL	DNL_{OUT}			0.95	LSB	$VDDA_{ADV}$,T_{ADV}
1.4.3.3	Output INL	INL_{OUT}			4	LSB	[3]
1.4.3.4	Output slew rate *	SR_{OUT}	0.1			V/µs	Voltage mode, C_L<20nF, using conditions of 1.4.3.1.
1.4.3.5	Short circuit current *	I_{OUT_max}	5	10	20	mA	
1.4.3.6	Addressable output signal range *	V_{OUT_ADR}	0		1	VDDA	2048 steps
1.4.4. PWM Output (Pin OUT, IO1)							
1.4.4.1	PWM high voltage	V_{PWM_H}	0.9			VDDA	R_L > 10 kΩ
1.4.4.2	PWM low voltage	V_{PWM_L}			0.1	VDDA	R_L > 10 kΩ
1.4.4.3	PWM output slew rate*	SR_{PWM}	15			V/µs	C_L < 1nF
1.4.5. Temperature Sensors (Pin IR_TEMP)							
1.4.5.1	Sensitivity external diode / resistor meas.	ST_{TS_E}	75		210	µV/LSB	At r_{ADC} = 13 Bit
1.4.6. Digital Outputs (IO1, IO2, OUT in digital mode)							
1.4.6.1	Output-High-Level	V_{DOUT_H}	0.9			VDDA	R_L > 1 kΩ
1.4.6.2	Output-Low-Level	V_{DOUT_L}			0.1	VDDA	R_L > 1 kΩ
1.4.6.3	Output Current *	I_{DOUT}	4			mA	

[1] Recommended bias adjust <= 4, notice application hints and power consumption adjust constraints in related application note
[2] Derated performance in lower part of supply voltage range (2.7 to 3.3V): 2.5 to 5%VDDA & 95 to 97.5%VDDA
[3] Output linearity and accuracy can be enhanced by additional analog output stage calibration
[4] Default configuration: 2nd order AD-conversion, 13Bit Resolution, gain >=210, fclk<=2.25MHz
* No measurement in mass production, parameter is guarantied by design and/or quality observatio

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
1.4.7. System Response							
1.4.7.1	Startup time [1],*	t_{STA}	2		5	ms	PowerOn to 1st measure result at output
1.4.7.2	Response time *	t_{RESP}	1.66	2.66	3.66	$1/f_{CON}$	66% jump, refer 2.3.4 for f_{CON}
1.4.7.3	Overall accuracy (deviation from ideal line including INL, gain and offset errors) [2],*	AC_{OUT}			0.10 0.25 0.50	% % %	T_{ADV} & $VDDA_{ADV}$ T_{AMB_TQA} & $VDDA_{ADV}$ @ current-loop-OUT & T_{ADV} & $VDDA_{ADV}$ (refer also application note AN05 of ZMD31050)
1.4.7.4	Analog Output Noise Peak-to-Peak *	$V_{NOISE,PP}$			10	mV	Shorted inputs, gain<=210 bandwidth ≤ 10kHz
1.4.7.5	Analog Output Noise RMS *	$V_{NOISE,RMS}$			3	mV	Shorted inputs, gain<=210 bandwidth ≤ 10kHz
1.4.7.6	Ratiometricity Error	RE_{OUT_5V} RE_{OUT_3V}			500 1000	ppm ppm	±5% respect. 1000ppm ±10% (5V) ±5% respect. 2000ppm ±10% (3V)

1.5. Interface Characteristics

Table 1.7. Interface Characteristics

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
1.5.1. Multiport Serial Interfaces (I^2C, SPI)							
1.5.1.1	Input-High-Level	$V_{I2C\_IN\_H}$	0.7		1	VDDA	
1.5.1.2	Input-Low-Level	$V_{I2C\_IN\_L}$	0		0.3	VDDA	
1.5.1.3	Output-Low-Level	$V_{I2C\_OUT\_L}$			0.1	VDDA	
1.5.1.4	Load capacitance @ SDA	C_{SDA}			400	pF	
1.5.1.5	Clock frequency SCL [3]	f_{SCL}			400	kHz	f_{CLK} ≥ 2MHz
1.5.1.6	Pull-up Resistor	R_{I2C_PU}	500			Ω	
1.5.1.7	Input capacitance (each pin)	C_{I2C_IN}			10	pF	valid for SPI as well
1.5.2. One Wire Serial Interface (ZACwire™)							
1.5.2.1	OWI start window	R_{OWI_PU}		20		ms	
1.5.2.2	Pull-up resistance master	R_{OWI_PU}	330			Ω	
1.5.2.3	OWI load capacitance	C_{OWI_LOAD}			0.08	t_{OWI_BIT} / R_{OWI_PU}	20µs < t_{OWI_BIT} < 100µs
1.5.2.4	Voltage level Low	V_{OWI_L}			0.2	VDDA	
1.5.2.5	Voltage level High	V_{OWI_H}	0.75			VDDA	

1 OWI – start window disabled, according default configuration (depends on resolution and configuration - start routine begins approximately 0.8ms after power on)
2 Accuracy better than 0.5% requires offset and gain calibration for the analog output stage, Parameter only for ratiometric output. Refer "ZMD31050_FunctionalDescription_Rev_*.pdf" for other output configurations.
3 Internal clock frequency fCLK has to be in minimum 5 times higher than communication clock frequency
* No measurement in mass production, parameter is guarantied by design and/or quality observatio

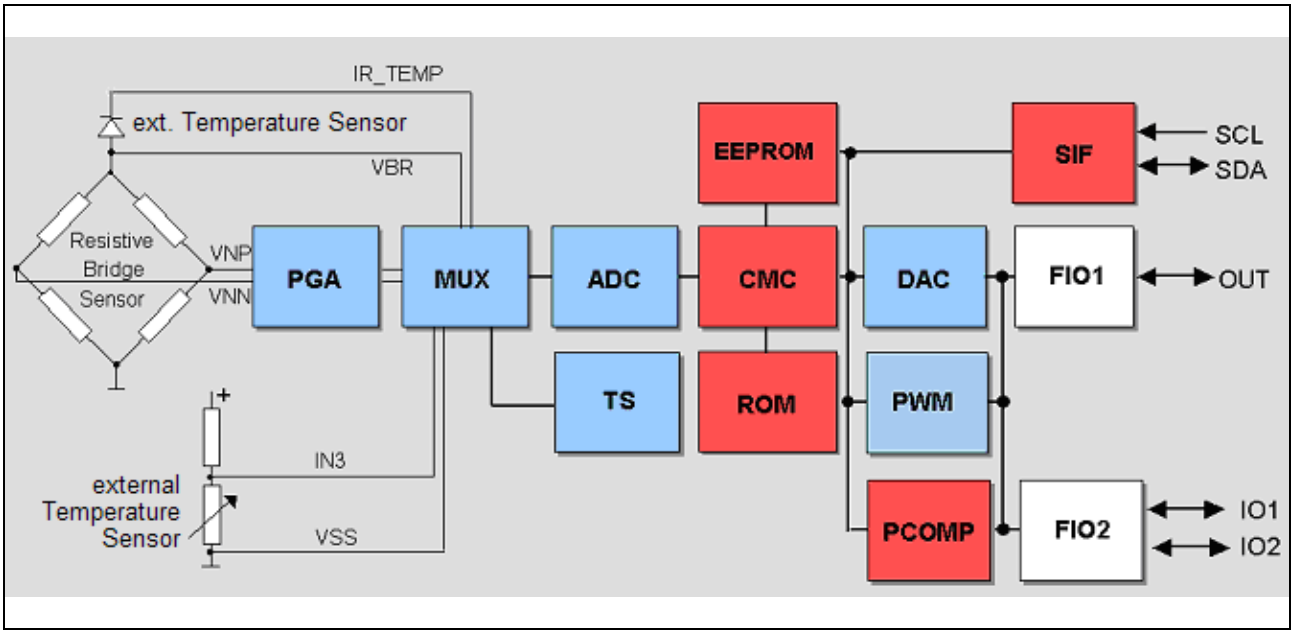
2 Circuit Description

2.1. Signal Flow

The ZMD31050's signal path is partly analog (blue) and partly digital (red). The analog part is realized differential – this means internal is the differential bridge sensor signal also handled via two signal lines, which are rejected symmetrically around a common mode potential (analog ground = VDDA/2).

Consequently it is possible to amplify positive and negative input signals, which are located in the common mode range of the signal input.

Figure 2.1 Block Diagram of the ZMD31050



PGA	Programmable gain amplifier
MUX	Multiplexer
ADC	Analog-to-digital converter
CMC	Calibration microcontroller
DAC	Digital-to-analog converter
FIO1	Flexible I/O 1: analog out (voltage/current), PWM2, ZACwire™ (one-wire-interface)
FIO2	Flexible I/O 2: PWM1, SPI data out, SPI slave select, Alarm1, Alarm2
SIF	Serial interface: I2C data I/O, SPI data in, clock
PCOMP	Programmable comparator
EEPROM	Non volatile memory for calibration parameters and configuration
TS	On-chip temperature sensor (pn-junction)
ROM	Memory for correction formula and –algorithm
PWM	PWM module

The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The Multiplexer (MUX) transmits the signals from bridge sensor, external diode or separate temperature sensor

to the ADC in a certain sequence (instead of the temperature diode the internal pn-junction (TS) can be used optionally). Afterwards the ADC converts these signals into digital values.

The digital signal correction takes place in the calibration micro-controller (CMC). It is based on a special correction formula located in the ROM and on sensor-specific coefficients (stored into the EEPROM during calibration). Dependent on the programmed output configuration the corrected sensor signal is output as analog value, as PWM signal or in digital format (SPI, I^2C, ZACwire^{TM}). The output signal is provided at 2 flexible I/O modules (FIO) and at the serial interface (SIF). The configuration data and the correction parameters can be programmed into the EEPROM via the digital interfaces.

The modular circuit concept enables fast custom designs varying these blocks and, as a result, functionality and die size.

2.2. Application Modes

For each application a configuration set has to be established (generally prior to calibration) by programming the on-chip EEPROM regarding to the following modes:

- Sensor channel
  - Sensor mode: ratiometric voltage or current supply mode.
  - Input range: The gain of the analog front end has to be chosen with respect to the maximum sensor signal span and to this has also adjusted the zero point of the ADC
  - Additional offset compensation: The extended analog offset compensation has to be enabled if required, e.g. if the sensor offset voltage is near to or larger than the sensor span.
  - Resolution/response time: The A/D converter has to be configured for resolution and conversion scheme (1st or 2nd order). These settings influence the sampling rate, signal integration time and this way the noise immunity.
  - Ability to invert the sensor bridge inputs
- Analog output
  - Choice of output method (voltage value, current loop, PWM) for output register 1.
  - Optional choice of additional output register 2: PWM via IO1 or alarm out module via IO1/2.
- **Digital communication**: The preferred protocol and its parameter have to be set.
- **Temperature**
  - The **temperature measure source** for the temperature correction has to be chosen.
  - The temperature measure source T1 sensor type for the temperature correction has to be chosen (only T1 is usable for correction!!!)
  - Optional: the **temperature measure channel** as the second output has to be chosen.
- **Supply voltage** : For non-ratiometric output the voltage regulation has to be configured.

Note: Not all possible combinations of settings are allowed (see section 2.5).

The calibration procedure must include
  - Set of coefficients of calibration calculation

and, depending on configuration,
  - Adjustment of the extended offset compensation,
  - Zero compensation of temperature measurement,
  - Adjustment of the bridge current

and, if necessary,
  - Set of thresholds and delays for the alarms and the reference voltage.

2.3. Analog Front End (AFE)

The analog front end consists of the programmable gain amplifier (PGA), the multiplexer (MUX) and the analog-to-digital converter (ADC).

2.3.1. Programmable Gain Amplifier (PGA)

The following tables show the adjustable gains, the processable sensor signal spans and the allowed common mode range.

Table 2.1 Adjustable gains, resulting sensor signal spans, and common mode ranges

No.	PGA Gain a_{IN}	Gain Amp1	Gain Amp2	Gain Amp3	Max. span V_{IN_SP} in mV/V	Input range V_{IN_CM} in % VDDA *
1	420	30	7	2	2	43 - 57
2	280	30	4,66	2	3	40 - 59
3	210	15	7	2	4	43 - 57
4	140	15	4,66	2	6	40 - 59
5	105	15	3,5	2	8	38 - 62
6	70	7,5	4,66	2	12	40 - 59
7	52,5	7,5	3,5	2	16	38 - 62
8	35	3,75	4,66	2	24	40 - 59
9	26,3	3,75	3,5	2	32	38 - 62
10	14	1	7	2	50	43 - 57
11	9,3	1	4,66	2	80	40 - 59
12	7	1	3,5	2	100	38 - 62
13	2,8	1	1,4	2	280	21 - 76

2.3.2. Extended Zero Point Compensation (XZC)

The ZMD31050 supports two methods of sensor offset cancellation (zero shift):

- Digital offset correction
- XZC – an analog cancellation for large offset values (up to approx 300% of span)

The digital sensor offset correction will be processed at the digital signal correction/conditioning by the CMC. The analog sensor offset pre-compensation will be needed for compensation of large offset values, which would be overdrive the analog signal path by uncompensated gaining. For analog sensor offset pre-compensation a compensation voltage will be added in the analog pre-gaining signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by 6 EEPROM bits. It allows an analog zero point shift up to 300% of the processable signal span.

The zero point shift of the temperature measurements can also be adjusted by 6 EEPROM bits (Z_{XZC}= -20…+20) and is calculated by:

$$V_{XZC} / VDD_{BR} = k * Z_{XZC} / (20 * a_{IN})$$

* Bridge in voltage mode, refer “ZMD31050 Functional description” for usable input signal/common mode range at bridge in current mode

Table 2.2 Extended Zero Point Compensation Range

PGA gain a_{IN}	Max. span V_{IN_SP} in mV/V	Calculation factor k	Offset shift per step in % full span	Approx. maximum offset shift in mV/V	Approx. maximum shift in [% V_{IN_SP}] (@ ± 20 steps)
420	2	3,0	15%	+/- 7	330
280	3	1,833	9%	+/- 6	200
210	4	3,0	15%	+/- 14	330
140	6	1,833	9%	+/- 12	200
105	8	1,25	6%	+/- 12	140
70	12	1,833	9%	+/- 24	200
52,5	16	1,25	6%	+/- 22	140
35	24	1,833	9%	+/-48	200
26,3	32	1,25	6%	+/- 45	140
14	50	3,0	15%	+/- 180	330
9,3	80	1,833	9%	+/- 160	200
7	100	1,25	6%	+/- 140	140
2,8	280	0,2	1%	+/- 60	22

Note: Z_{XZC} can be adjusted in range –31 to 31, parameters are guaranteed only in range –20 to 20.

2.3.3. Measurement Cycle realized by Multiplexer

The Multiplexer selects, depending on EEPROM settings, the following inputs in a certain sequence.

- Internal offset of the input channel measured by input short circuiting
- Bridge temperature signal measured by external and internal diode (pn-junction)
- Bridge temperature signal measured by bridge resistors → Start routine
- Temperature measurement by external thermistor
- Pre-amplified bridge sensor signal

The complete measurement cycle is controlled by the CMC. The cycle diagram at the right shows its principle structure.

The EEPROM adjustable parameters are:

- Pressure measurement count, PMC=<1,2,4,8,16,32,64,128>
- Temperature 2 measurement enable, T2E=<0,1>

After Power ON the start routine is called. It contains the pressure and auto zero measurement. When enabled it measures the temperature and its auto zeros.

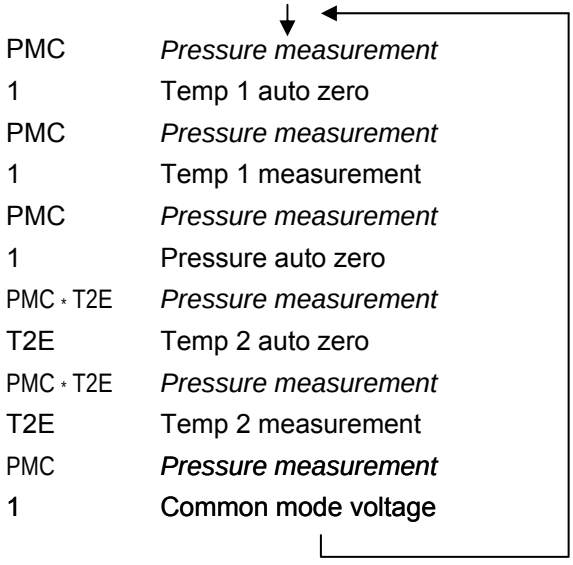


Figure 2.2. Measurement cycle ZMD31050

2.3.4. Analog-to-Digital Converter

The ADC is a charge balancing converter in full differential switched capacitor technique. It can be used as first or second order converter:

In the **first order** mode it is inherently monotone and insensitive against short and long term instability of the clock frequency. The conversion cycle time depends on the desired resolution and can be roughly calculated by:

$$t_{CYC\_1} = 2^{r_{ADC}}\ \mu s$$

The available ADC-resolutions are r_{ADC} = <9,10,11,12,13,14>.

In the **second order** mode two conversions are stacked with the advantage of much shorter conversion cycle time and the drawback of a lower noise immunity caused by the shorter signal integration period. The conversion cycle time at this mode is roughly calculated by:

$$t_{CYC\_2} = 2^{(r_{ADC}+3)/2}\ \mu s$$

The available ADC-resolutions are r_{ADC} = <11,12,13,14,15>.

The result of the AD conversion is a relative counter result corresponding to the following equation:

$$Z_{ADC} = 2^{r_{ADC}} * [(V_{ADC\_DIFF}/V_{ADC\_REF}) + (1 - RS_{ADC})]$$

Z_{ADC}: Number of counts (result of the conversion)

V_{ADC_DIFF}: Differential input voltage of ADC (= a_{IN} * V_{IN_DIFF})

V_{ADC_REF}: Reference voltage of ADC (= VBR or VDDA)

RS_{ADC}: Digital ADC Range Shift (RS_{ADC} = $^{15}/_{16}$, $^{7}/_{8}$, $^{3}/_{4}$, $^{1}/_{2}$, controlled by the EEPROM content)

With the RS_{ADC} value a sensor input signal can be shifted in the optimal input range of the ADC.

The Pin <VBR>-potential is used in “VBR=VREF” mode as AD converters reference voltage V_{ADC_REF}. Sensor bridges with no ratiometric behaviour (f.i. temperature compensated bridges), which are supplied by a constant current, requires VDDA potential as V_{ADC_REF} and this can be adjusted by in configuration. If these mode is enabled, XZC can’t by used (adjustment=0), but it has to be enabled (refer calculation sheet “ZMD31050_Bridge_Current_Excitation_Rev*.xls” for details).

Note: The AD conversion time (sample rate) is only a part of a whole signal conditioning cycle.

Table 2.3 Output Resolution versus Sample Rate

ADC	Maximum Output Resolution				Sample Rate f_{CON}	
Order	r_{ADC} [1]	Digital-OUT	Analog-OUT	r_{PWM}	f_{CLK}=2MHz	f_{CLK} =2.25MHz
O_{ADC}	Bit	Bit	Bit	Bit	Hz	Hz
1	9	9	9	9	1302	1465
1	10	10	10	10	781	879
1	11	11	11	11	434	488
1	12	12	11	12	230	259

[1] *ADC Resolution should be 1 to 2 Bits higher then applied Output Resolution*

ADC	Maximum Output Resolution				Sample Rate f_{CON}	
Order	r_{ADC} [1]	Digital-OUT	Analog-OUT	r_{PWM}	f_{CLK}=2MHz	f_{CLK} =2.25MHz
O_{ADC}	Bit	Bit	Bit	Bit	Hz	Hz
1	13	13	11	12	115	129
1	14	14	11	12	59	67
2	10	10	10	10	3906	4395
2	11	11	11	11	3906	4395
2	12	12	11	12	3906	4395
2	13	13	11	12	1953	2197
2	14	14	11	12	1953	2197
2	15	15	11	12	977	1099

2.4. System Control

The system control has the following features:

- Control of the I/O relations and of the measurement cycle regarding to the EEPROM-stored configuration data
- 16 bit correction calculation for each measurement signal using the EEPROM stored calibration coefficients and ROM-based algorithms
- Started by internal POC, internal clock – generator or external clock
- For safety improvement the EEPROM data are proved with a signature within initialization procedure, the registers of the CMC are steadily observed with a parity check. Once an error is detected, the error flag of the CMC is set and the outputs are driven to a diagnostic value

Note: *The conditioning includes up to third order sensor input correction. The available adjustment ranges depend on the specific calibration parameters, a detailed description will be issued later. To give a rough idea: Offset compensation and linear correction are only limited by the loose of resolution it will cause, the second order correction is possible up to about 20% full scale difference to straight line, third order up to about 10% (ADC resolution = 13bit). The temperature calibration includes first and second order correction and should be fairly sufficient in all relevant cases. ADC resolution influences also calibration possibilities – 1 bit more resolution reduces calibration range by approximately 50%.*

[1] *ADC Resolution should be 1 to 2 Bits higher then applied Output Resolution*

2.5. Output Stage

Table 2.4. Output configurations overview

	Used SIF		Used I/O pins			
No.	**I2C**	**SPI**	**OUT**	**IO1**	**IO2**	**SDA**
1	X					Data I/O
2	X			ALARM1		Data I/O
3	X				ALARM2	Data I/O
4	X			ALARM1	ALARM2	Data I/O
5	X			PWM1		Data I/O
6	X			PWM1	ALARM2	Data I/O
7	X		Analog			Data I/O
8	X		Analog	ALARM1		Data I/O
9	X		Analog		ALARM2	Data I/O
10	X		Analog	ALARM1	ALARM2	Data I/O
11	X		Analog	PWM1		Data I/O
12	X		Analog	PWM1	ALARM2	Data I/O
13	X		PWM2			Data I/O
14	X		PWM2	ALARM1		Data I/O
15	X		PWM2		ALARM2	Data I/O
16	X		PWM2	ALARM1	ALARM2	Data I/O
17	X		PWM2	PWM1		Data I/O
18	X		PWM2	PWM1	ALARM2	Data I/O
19		X		Data out	Slave select	Data in
20		X		Data out ALARM1	Slave select -	Data in -
21		X		Data out PWM1	Slave select -	Data in -
22		X	Analog	Data out	Slave select	Data in
23		X	Analog	Data out ALARM1	Slave select -	Data in -
24		X	Analog	Data out PWM1	Slave select -	Data in -
25		X	PWM2	Data out	Slave select	Data in
26		X	PWM2	Data out ALARM1	Slave select -	Data in -
27		X	PWM2	Data out PWM1	Slave select -	Data in -

The ZMD31050 provides the following I/O pins: OUT, IO1, IO2 and SDA.

Via these pins the following signal formats can be output: Analog (voltage/current), PWM, Data (SPI/I^2C), Alarm.

The following values can be provided at the O/I pins: bridge sensor signal, temperature signal 1, temperature signal 2, alarm.

Note:

The Alarm signal only refers to the bridge sensor signal, but never to a temperature signal.

Due to the necessary pin sharing there are restrictions to the possible combinations of outputs and interface connections.

The table beside gives an overview about possible combinations.

Note:

In the SPI mode the pin IO2 is used as Slave select. Thus no Alarm 2 can be output in this mode.

2.5.1. Analog Output

For the analog output 3 registers of 15 bit depth are available, which can store the actual pressure and the results of temperature measurement 1 and 2. Each register can be independently switched to one of two output slots connected to the Pin OUT and IO1 respectively. In these output slots different output modules are available according to the following table:

Table 2.5. Analog output configuration

Output slot:	OUT	IO1
Voltage	x	
PWM	x	x

The voltage module consists of an 11bit resistor string – DAC with buffered output and a subsequent inverting amplifier with class AB rail-to-rail OpAmp. The two feedback nets are connected to the Pins FBN and FBP. This structure offers wide flexibility for the output configuration, for example voltage output and 4 mA to 20 mA current loop output. To short circuit the analog output against VSS or VDDA does not damage the ZMD31050.

The PWM module provides pulse streams with signal dependent duty cycle. The PWM – frequency depends on resolution and clock divider. The maximum resolution is 12 bit, the maximum PWM – frequency is 4 kHz (9 bit). If both, second PWM and SPI protocol are activated, the output pin IO1 is shared between the PWM output and the SPI_SDO output of the serial interface (interface communication interrupts the PWM output).

2.5.2. Comparator Module (ALARM Output)

The comparator module consists of two comparator channels connectable to IO1 and IO2 respectively. Each of them can be independently programmed referring to the parameters threshold, hysteresis, switching direction and on/off – delay. Additional a window comparator mode is available.

2.5.3. Serial Digital Interface

The ZMD31050 includes a serial digital interface which is able to communicate in three different communication protocols – I^2C^{TM}, SPI^{TM} and $ZACwire^{TM}$ (one wire communication).

In the SPI mode the pin IO2 operates as slave select input, the pin IO1 as data output.

Initializing Communication

After power-on the interface is for about 20ms (start window) in the state ZACwire. During the start window it is possible to communicate via the one wire interface (pin OUT).

Detecting a proper request inside the start window the interface stays in the state ZACwire. This state can be left by certain commands or a new power-on.

If during the start window no request happens then the serial interface switches to I^2C or SPI mode (depending on EEPROM settings). The OUT pin is used as analog output or as PWM output (also depending on EEPROM settings). The start window can generally be disabled (or enabled) by a special EEPROM setting.

For detailed description of the serial interfaces see “ZMD31050 Functional Description”.

2.6. Voltage Regulator

For ratiometric applications 3V to 5V (±10%) the external supply voltage can be used for sensor element biasing. If an absolute analog output is desired then the internal voltage regulator with external power regulation element (JFET) can be used. The regulation is bandgap reference based and designed for an external supply voltage V_{SUPP} in the range of 7V to 40VDC. The internal supply and sensor bridge voltage can be varied between 3V and 5.5V in 4 steps with the voltage regulator.

2.7. Watchdog and Error Detection

The ZMD31050 detects various possible errors. A detected error is signalized by changing in a diagnostic mode. In this case the analog output is set to the high or low level (maximum or minimum possible output value) and the output registers of the digital serial interface are set to a significant error code.

A watchdog oversees the continuous working of the CMC and the running measurement loop.

A check of the sensor bridge for broken wires is done permanently by two comparators watching the input voltage of each input [(VSSA + 0.5V) to (VDDA – 0.5V)]. Add on the common mode voltage of the sensor is watched permanently (sensor aging).

Different functions and blocks in digital part are watched like RAM-, ROM,- EEPROM- and Register content continuously, the document “ZMD31050 Functional Description” contains in chapter 1.3.4 a detailed description of all watched blocks and methods of messaging of errors.

3 Application Circuit Examples

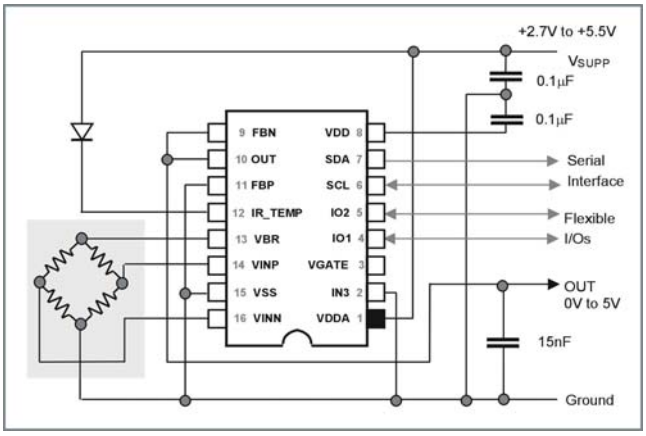


Figure 3.1 Example 1

Typical ratiometric measurement with voltage output, temperature compensation via external diode, internal VDD regulator and active sensor connection check (bridge must not be at VDDA)

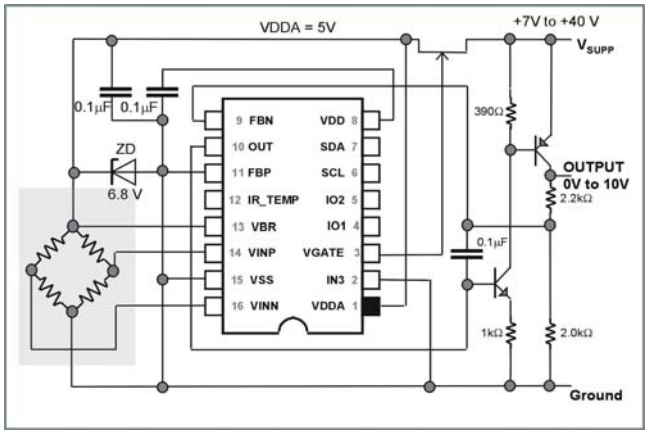


Figure 3.2 Example 2

0V to 10V output configuration, supply regulator (external JFET), temperature compensation via internal diode and bridge in voltage mode

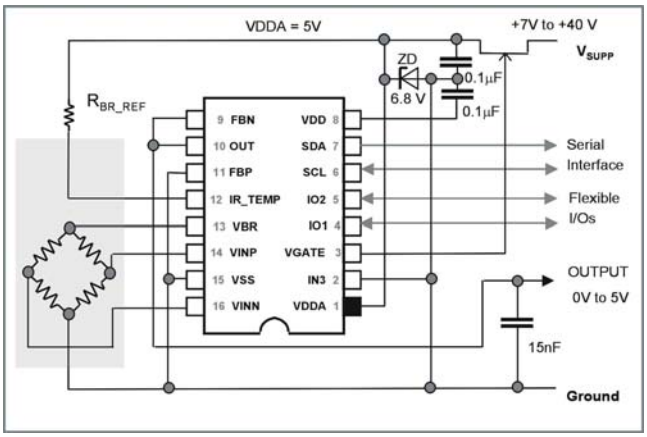


Figure 3.3 Example 3

Absolute voltage output, supply regulator (external JFET), constant current excitation of the sensor bridge, temperature compensation by bridge voltage drop measurement, internal VDD regulator without ext. capacitor

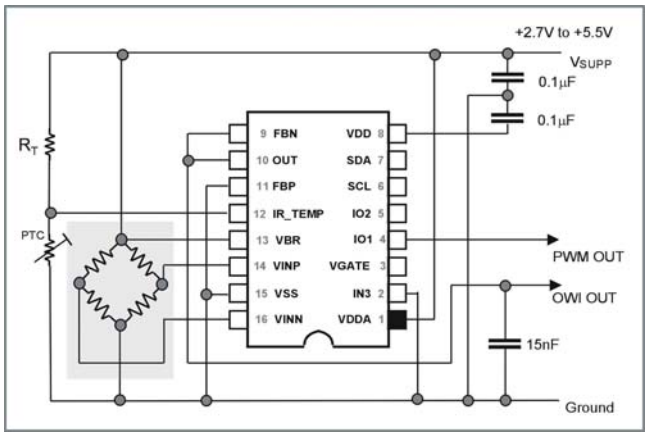


Figure 3.4 Example 4

Ratiometric bridge differential signal measurement, 3–wire connection for end of line calibration at pin OUT (ZACwire™), additional temperature measurement with external thermistor and PWM-output at pin IO1

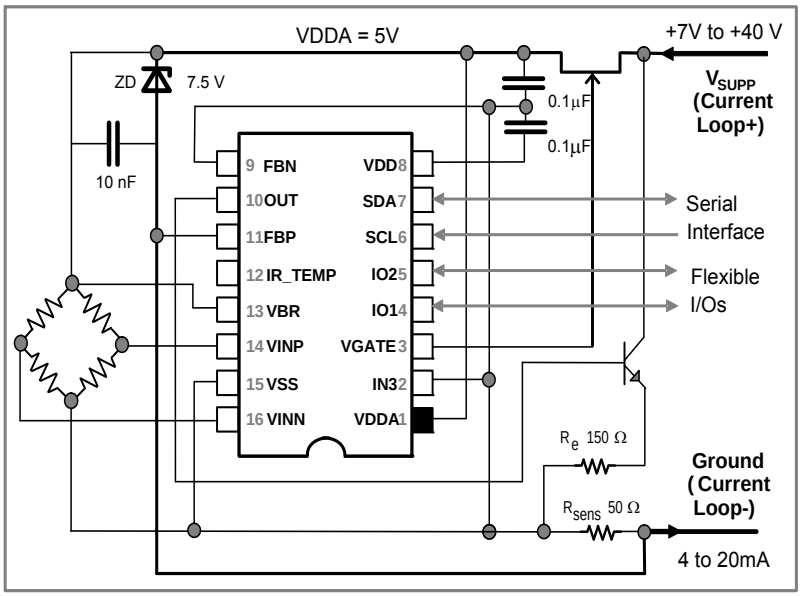


Figure 3.5 Example 5
Two-wire-(4 to 20) mA configuration [(7 to 40) V], temperature compensation via internal diode

Hints: It is possible to combine or split connectivity of different application examples. For VDD generation ZMDI recommends to use internal supply voltage regulator with external capacitor. Notice additional application notes for usage of supply voltage regulation property (non ratiometric mode) and current loop output mode.

4 ESD/Latch-Up-Protection

All pins have an ESD protection of >2000V (except the pins INN, INP and FBP with > 1200V) and a latch-up protection of ±100mA or of +8V/ –4V (to VSS/VSSA) – refer chapter 5 for details and restrictions. ESD protection referred to the human body model is tested with devices in SSOP16 packages during product qualification. The ESD test follows the human body model with 1.5kOhm/100pF based on MIL 883, method 3015.7.

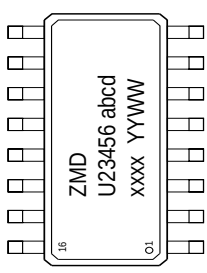
5 Pin Configuration and Package

Table 5.1. Pin Configuration

Pin	Name	Description	Remarks	Latch-Up related Application Circuit Restrictions and/or Remarks
1	VDDA	Positive analog supply voltage	Supply	
2	IN3	Resistive temp sensor IN & external clock IN	Analog IN	Free accessible (latch-up related)
3	VGATE	Gate voltage for external regulator FET	Analog OUT	Only connection to external FET
4	IO1	SPI data out & ALARM1 & PWM1 Output	Digital IO	Free accessibility
5	IO2	SPI chip select & ALARM2	Digital IO	Free accessibility
6	SCL	I²C clock & SPI clock	Digital IN, pull-up	Free accessibility
7	SDA	Data IO for I²C & data IN for SPI	Digital IO, pull-up	Free accessibility
8	VDD	Positive digital supply voltage	Supply	Only capacitor to VSS allowed, otherwise no application access
9	FBN	Negative feedback connection output stage	Analog IO	Free accessibility
10	OUT	Analog output & PWM2 Output & one wire interface i/o	Analog OUT & dig. IO	Free accessibility
11	FBP	Positive feedback connection output stage	Analog IO	Free accessibility
12	IR_TEMP	Current source resistor i/o & temp. diode in	Analog IO	Circuitry secures potential inside of VSS-VDDA range, otherwise no application access
13	VBR	Bridge top sensing in bridge current out	Analog IO	Only short to VDDA or connection to sensor bridge, otherwise no application access
14	VINP	Positive input sensor bridge	Analog IN	Free accessibility
15	VSS	Negative supply voltage	Ground	
16	VINN	Negative input sensor bridge	Analog IN	Free accessibility

The standard package of the ZMD31050 is a SSOP16 (5.3mm body width) with lead-pitch 0.65mm:

Figure 5.1. Pin Configuration



Pin-Nr	Pin-Name	Pin-Name	Pin-Nr
9	FBN	VDD	8
10	OUT	SDA	7
11	FBP	SCL	6
12	IR_TEMP	IO2	5
13	VBR	IO1	4
14	VINP	VGATE	3
15	VSS	IN3	2
16	VINN	VDDA	1

6 Reliability

A reliability investigation according to the in-house non-automotive standard will be performed.

A fit rate < 5fit (temp=55°C, S=60%) is guaranteed. A typical fit rate of the C7A-technologie, which is used for ZMD30150, is 2.5fit .

7 Customization

For high-volume applications, which require an up- or downgraded functionality compared to the ZM31050, ZMDI can customize the circuit design by adding or removing certain functional blocks.

For it ZMDI has a considerable library of sensor-dedicated circuitry blocks.

Thus ZMDI can provide a custom solution quickly. Please contact ZMDI for further information.

8 Related Documents

Document	File Name
ZMD31050 Feature Sheet	*ZMD31050_Feature_Sheet_rev_x_yy.pdf*
ZMD31050 Functional Description	*ZMD31050_FunctionalDescription_rev_x_yy.pdf*
ZMD31050 Evaluation Kit Description	*ZMD31050_Application_Kit_Description_rev_x_yy.pdf*
ZMD31050 Development Status Report (including parts identification table)	
ZMD31050 Application Notes	

Visit ZMDI's website www.zmdi.com or contact your nearest sales office for the latest version of these documents.

9 Document Revision History

Revision	Date	Description
1.00	-	First release of document.
1.01	-	Headlines and footnotes at all pages updated
1.02	-	5.5.1.7 – Input capacitance of digital interface pins added
1.03	-	5.4 – note 4 “Default Configuration” added 5.4.7.3 – overall accuracy / values & conditions for current loop output inserted 6. – Reliability / fit rate values added
1.04	September 2009	adjust to new ZMDI template
1.05	October 2009	changed “Related Documents” and “Document Revision History” so that information is included in table change to ZMDI denotation

Sales Offices and Further Information

www.zmdi.com

ZMD AG
Grenzstrasse 28
01109 Dresden
Germany

Phone +49 (0)351.8822.7.772
Fax +49(0)351.8822.87.772
sales@zmdi.com

ZMD America, Inc.
201 Old Country Road
Suite 204
Melville, NY 11747
USA

Phone +01 (631) 549-2666
Fax +01 (631) 549-2882
sales@zmdi.com

ZMD Japan
2nd Floor, Shinbashi Tokyu Bldg.
4-21-3, Shinbashi, Minato-ku
Tokyo, 105-0004
Japan

Phone +81.3.6895.7410
Fax +81.3.6895.7301
sales@zmdi.com

ZMD Far East
3F, No.,51, Sec. 2,
Keelung Road
11052 Taipei
Taiwan

Phone +886.3.563.1388
Fax +886.3.563.6385
sales@zmdi.com